IN THE CLAIMS

Please amend the claims to read as follows:

1. (Currently Amended) A semiconductor device comprising:

at least three power terminals provided one above the other; and

at least one semiconductor chip having a first main surface and a second main surface opposite and parallel to the first main surface, said first and second main surfaces being sandwiched between and in parallel with a predetermined two power terminals of said at least three power terminals, such that the first and second main surfaces of the at least one semiconductor chip are electrically connected to the predetermined two power terminals ~~without bonding wires~~ by soldering or pressure welding.

2. (Previously Presented) The semiconductor device according to claim 1, wherein the uppermost one and lowermost one of said at least three power terminals extend in the same direction.

3. (Previously Presented) The semiconductor device according to claim 2, wherein a power terminal positioned at the middle among said at least three power terminals extends in a direction opposite to or perpendicular to the uppermost one or lowermost one of said at least three power terminals.

4. (Currently Amended) The semiconductor device according to claim 1, wherein ~~one face of said at least one semiconductor chip interposed between said two power terminals is connected to one power terminal of said two power terminals by soldering or pressure welding, and another face~~ the second main surface is connected to ~~another power terminal of~~

~~said~~ one of the predetermined two power terminals ~~by soldering or pressure welding~~ through a buffer plate.

5. (Previously Presented) The semiconductor device according to claim 1, wherein two currents flow in opposite directions in said uppermost one and lowermost one of said at least three power terminals, while said at least one semiconductor chip is operating.

6. (Previously Presented) The semiconductor device according to claim 1, wherein said at least one semiconductor chip interposed between said two power terminals includes a plurality of semiconductor chips, and at least one insulation layer is provided between said plurality of semiconductor chips.

7. (Previously Presented) The semiconductor device according to claim 6, wherein said plurality of semiconductor chips includes at least one transistor and at least one diode, and wherein at least one control electrode is connected to said at least one transistor to control said at least one transistor.

8. (Previously Presented) The semiconductor device according to claim 7, wherein said at least one transistor has a control electrode pad, said control electrode is connected to said control electrode pad by wire bonding or by interposing a buffer plate between said control electrode and said control electrode pad.

9. (Previously Presented) The semiconductor device according to claim 7, wherein said control electrode is led out in a direction opposite to or perpendicular to the uppermost one or lowermost one of said at least three power terminals.

10. (Previously Presented) The semiconductor device according to claim 4, wherein the uppermost one and lowermost one of said at least three power terminals have a screw fixing structure so as to connect said at least one semiconductor chip by pressure welding between said two power terminals.

11. (Currently Amended) A semiconductor device comprising:

at least three power terminals provided one above another; and

at least one semiconductor chip having a first main surface and a second main surface opposite and parallel to the first main surface, said first and second main surfaces being sandwiched between and in parallel with a predetermined two power terminals of said at least three power terminals, such that the first and second main surfaces of the at least one semiconductor chip are electrically connected to the two power terminals ~~without bonding wires~~,

wherein the first main surface of said at least one semiconductor chip interposed between said two power terminals is connected to one power terminal of said two power terminals by soldering or pressure welding, and the second main surface is connected to another power terminal of said two power terminals by soldering or pressure welding.

12. (Previously Presented) The semiconductor device according to claim 11, wherein the uppermost one and lowermost one of said at least three power terminals extend in the same direction.

13. (Previously Presented) The semiconductor device according to claim 12, wherein a power terminal positioned at the middle among said at least three power terminals extends

in a direction opposite to or perpendicular to the uppermost one or lowermost one of said at least three power terminals.

14. (Previously Presented) The semiconductor device according to claim 11, wherein two currents flow in opposite directions in said uppermost one and lowermost one of said at least three power terminals, while said at least one semiconductor chip is operating.

15. (Previously Presented) The semiconductor device according to claim 11, wherein said at least one semiconductor chip interposed between said two power terminals includes a plurality of semiconductor chips, and at least one insulation layer is provided between said plurality of semiconductor chips.

16. (Previously Presented) The semiconductor device according to claim 15, wherein said plurality of semiconductor chips includes at least one transistor and at least one diode, and wherein at least one control electrode is connected to said at least one transistor to control said at least one transistor.

17. (Previously Presented) The semiconductor device according to claim 16, wherein said at least one transistor has a control electrode pad, said control electrode is connected to said control electrode pad by wire bonding or by interposing a buffer plate between said control electrode and said control electrode pad.

18. (Previously Presented) The semiconductor device according to claim 16, wherein said control electrode is led out in a direction opposite to or perpendicular to the uppermost one or lowermost one of said at least three power terminals.

19. (Previously Presented) The semiconductor device according to claim 11, wherein the uppermost one and lowermost one of said at least three power terminals have a screw fixing structure so as to connect said at least one semiconductor chip by pressure welding between said two power terminals.